GaN for energy efficiency in power electronics

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The Challenge	• What problem are we trying to solve?
The Science	• Why GaN?
The Engineering	• Those trade-offs.
The Market	• Show me the money

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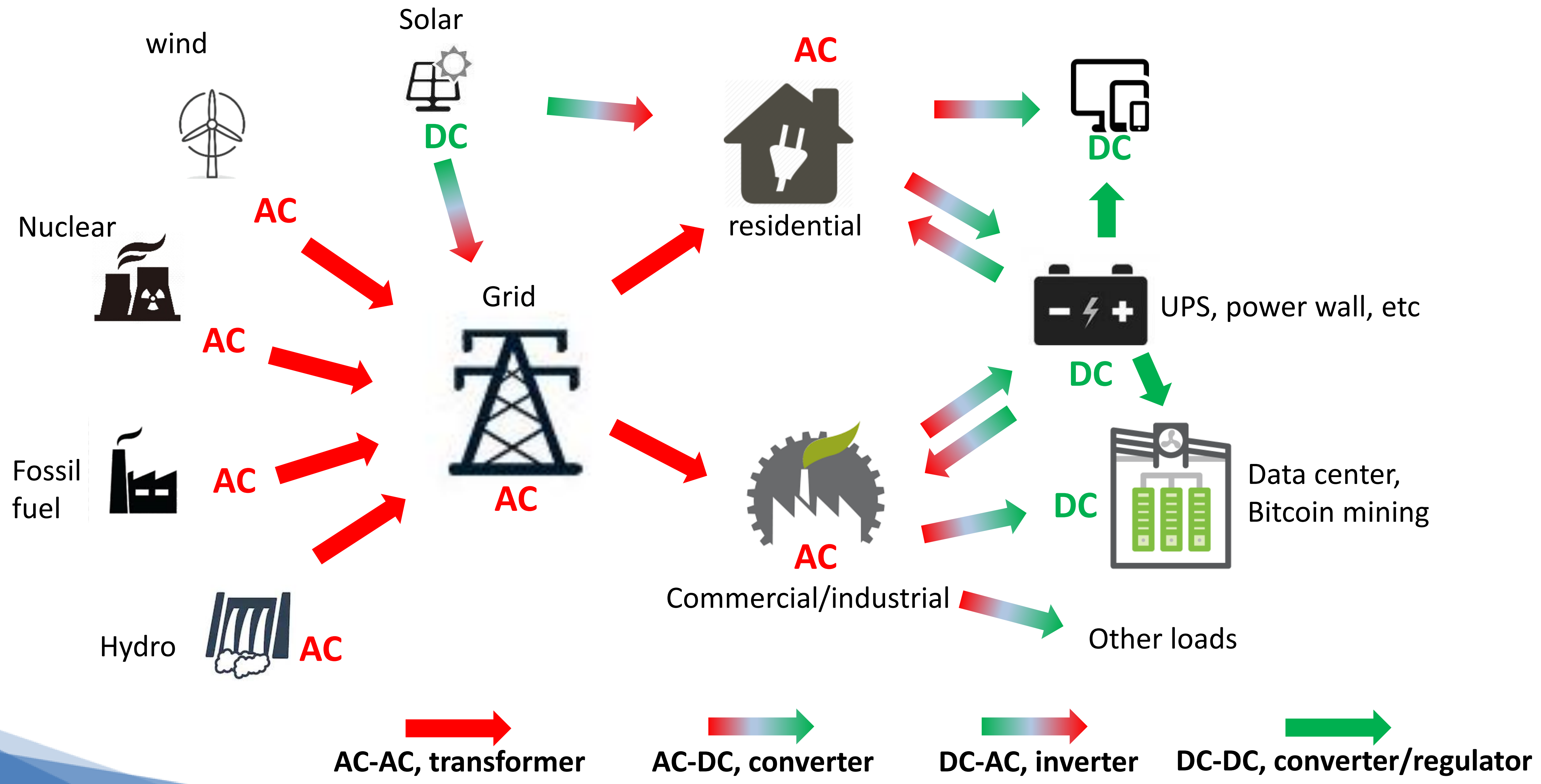
A simplified map of electricity flow



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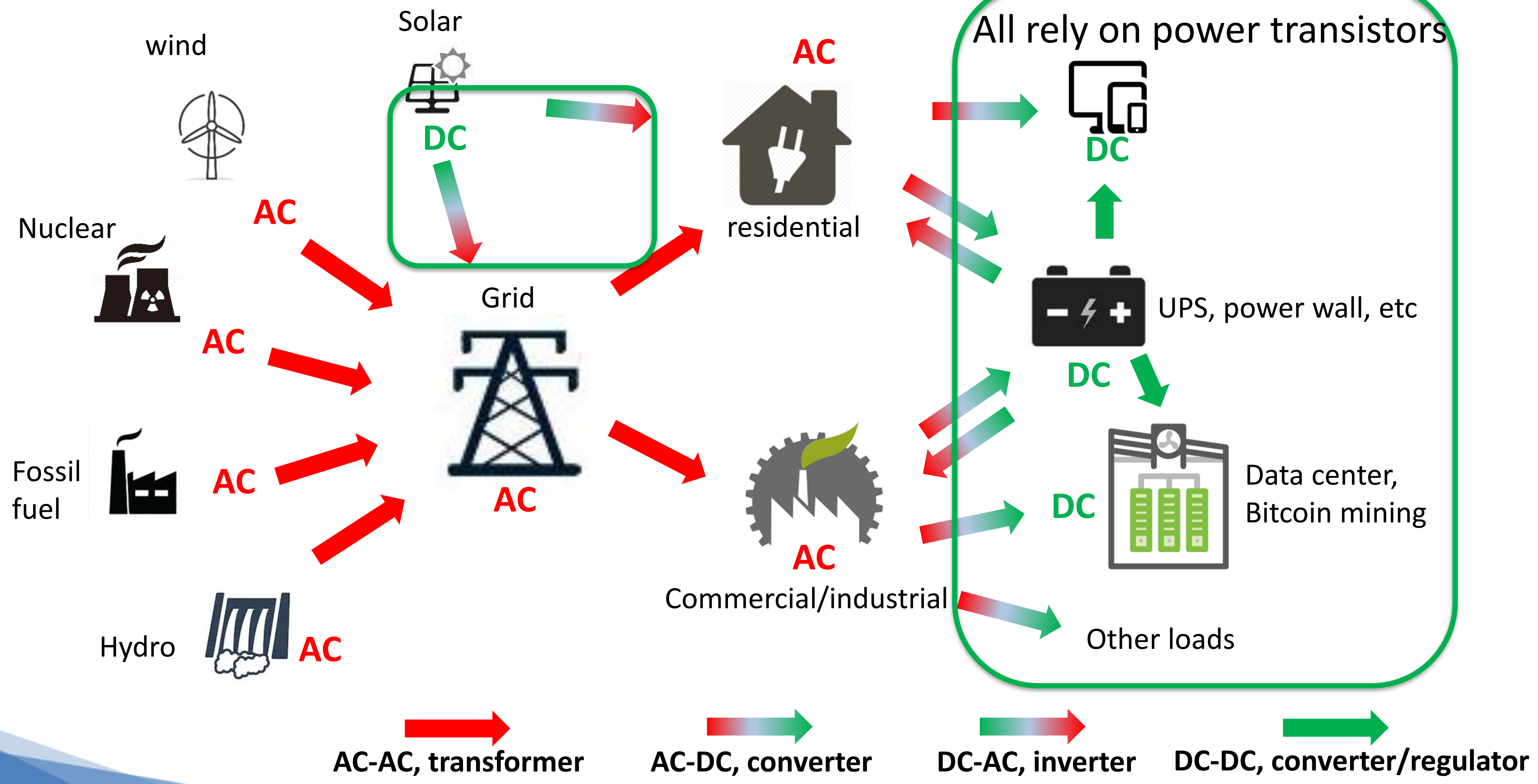
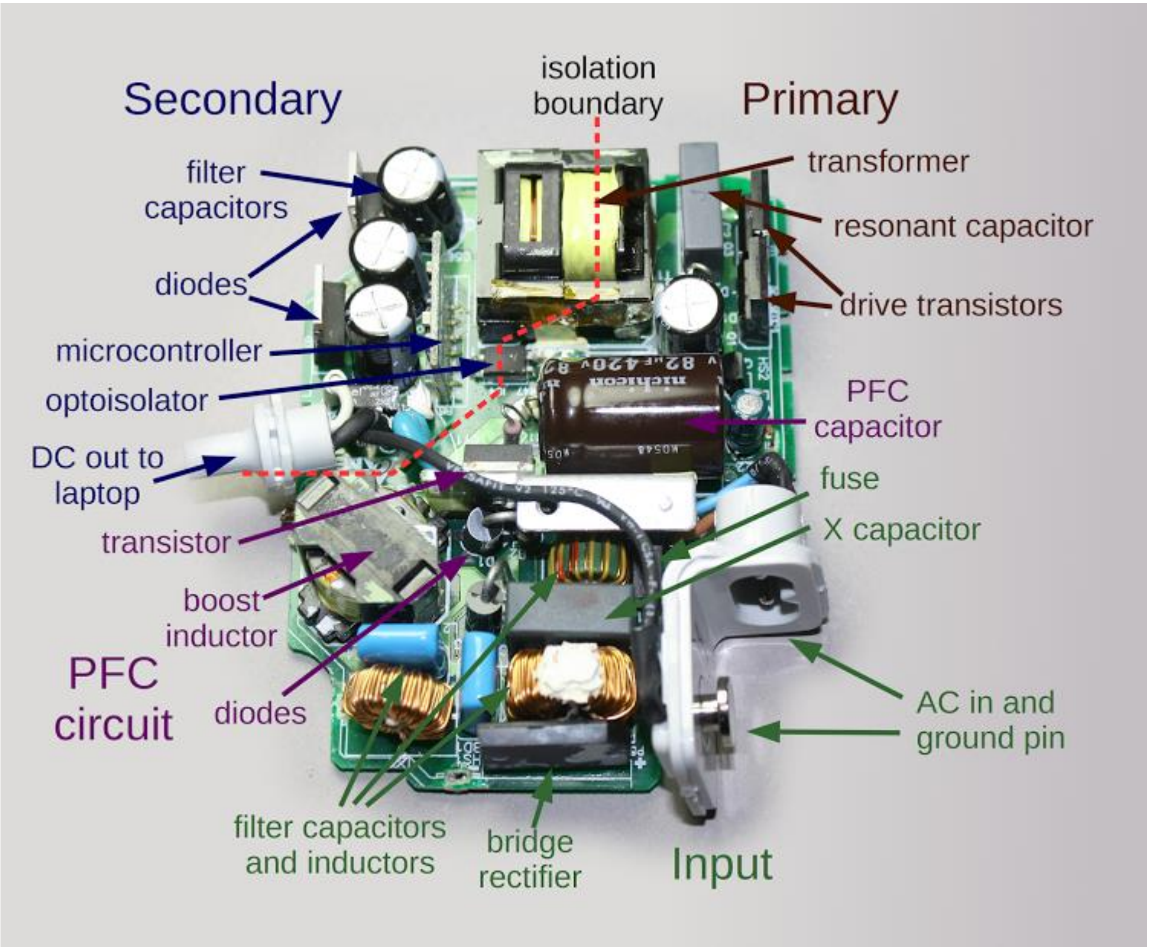


A simple converter device



Input AC high V, low F

↓ Bridge rectifier, PFC circuit

DC high V

↓ Primary drive transistors

AC high V, high F

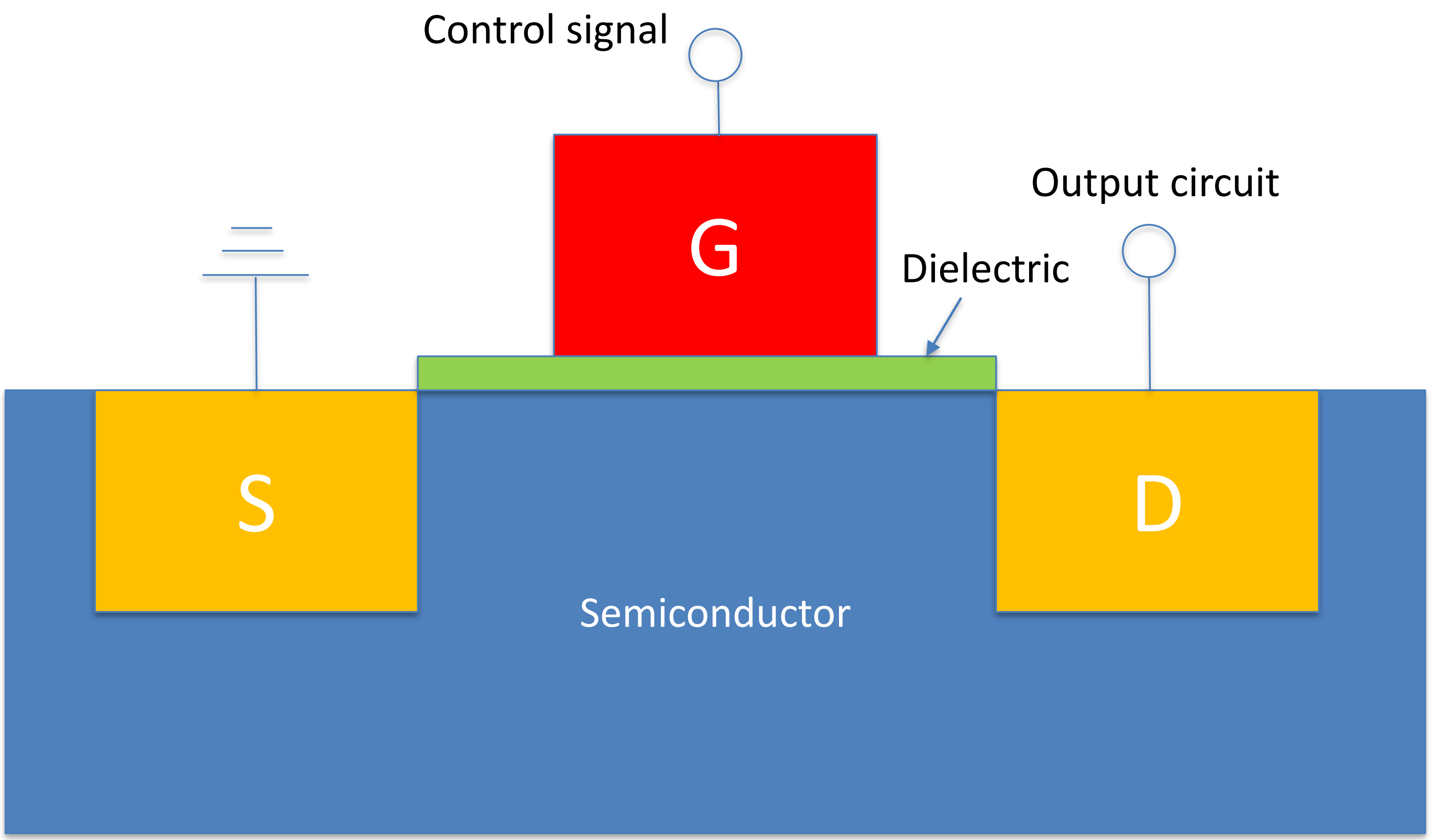
↓ transformer

AC low V, high F

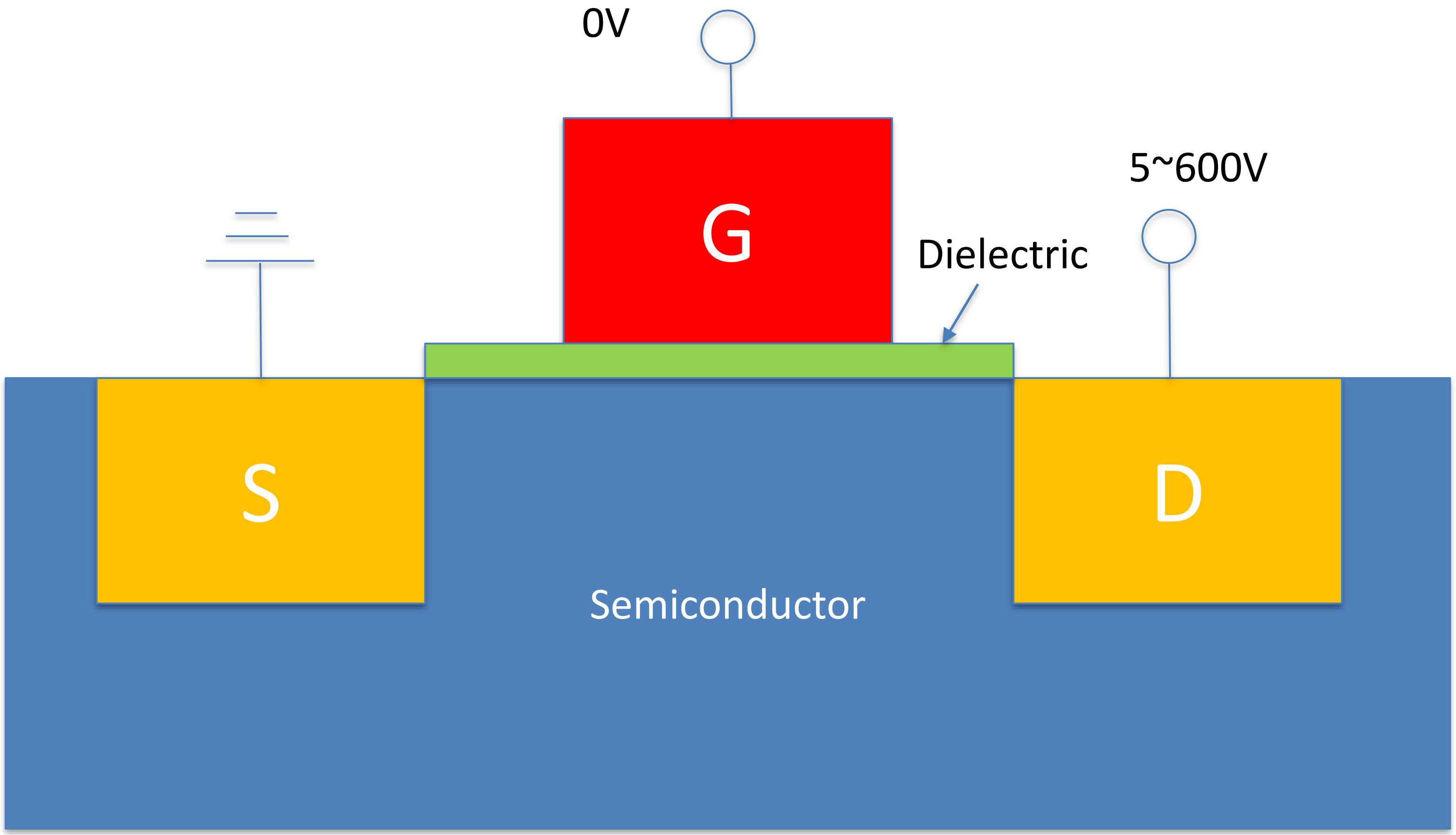
↓ Diodes

DC low V

How does a transistor work/waste energy



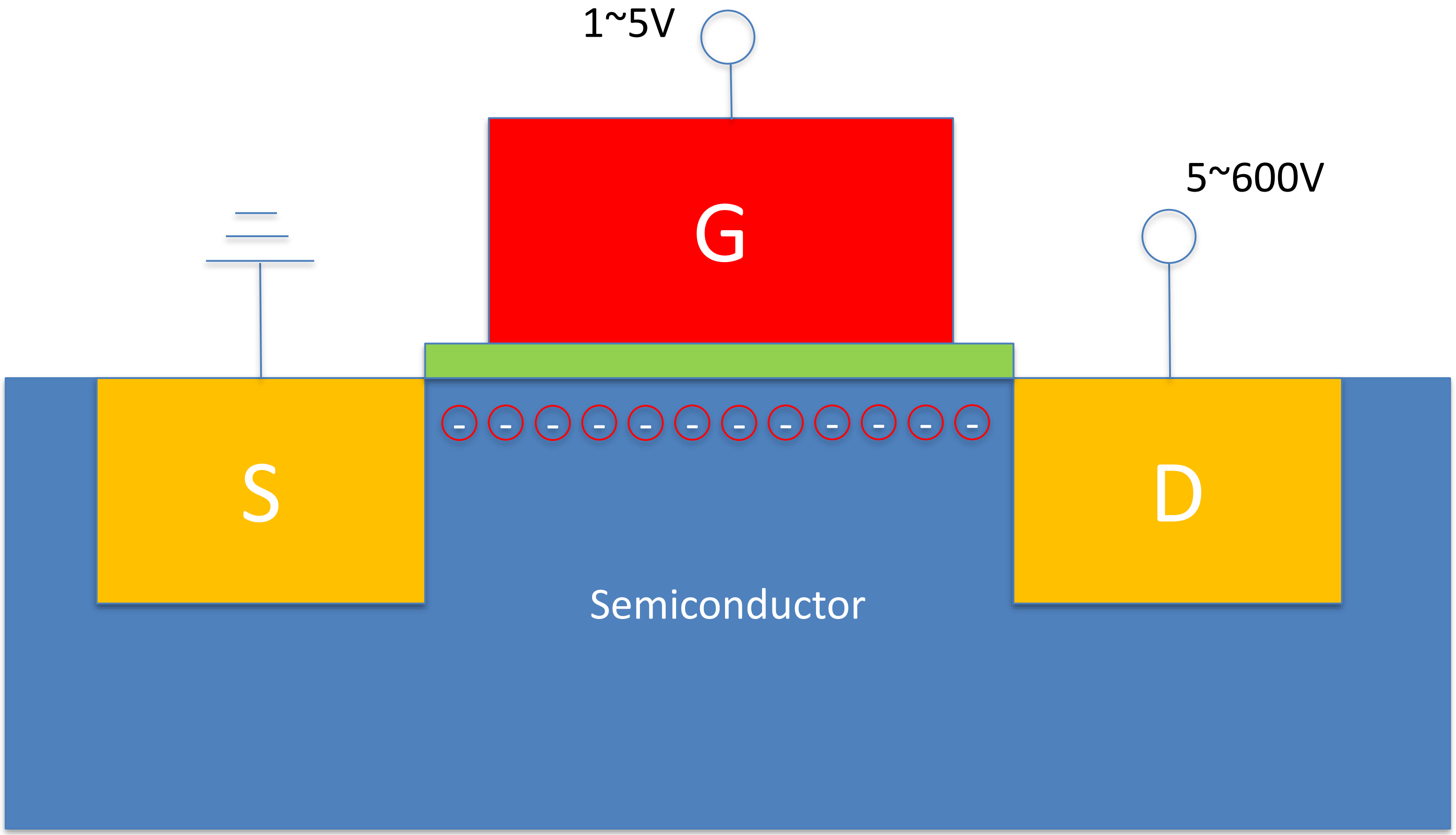
How does a transistor work/waste energy



OFF

- Vg<Vth
- Low electron density under the gate,
- High Rsd
- Fixed Vsd
- Low Isd
- Energy waste from leakage of Isd and Igs.

How does a transistor work/waste energy



ON

- Vg>Vth
- Low electron density under the gate,
- Low Rsd
- Fixed Vsd
- high Isd
- Energy waste from Rsd.

When switching at high frequency, the gate capacitance also consume energy.

Towards a higher efficiency

- Lower Ron loss
  - Reduce channel distance(semiconductor breakdown)
  - Increase doping density(limited, causing lower mobility)
  - Switch to a high electron mobility material.
- Lower gate capacitance loss
  - Shorter gate(more S to D leakage)
  - Lower gate voltage (not easy)

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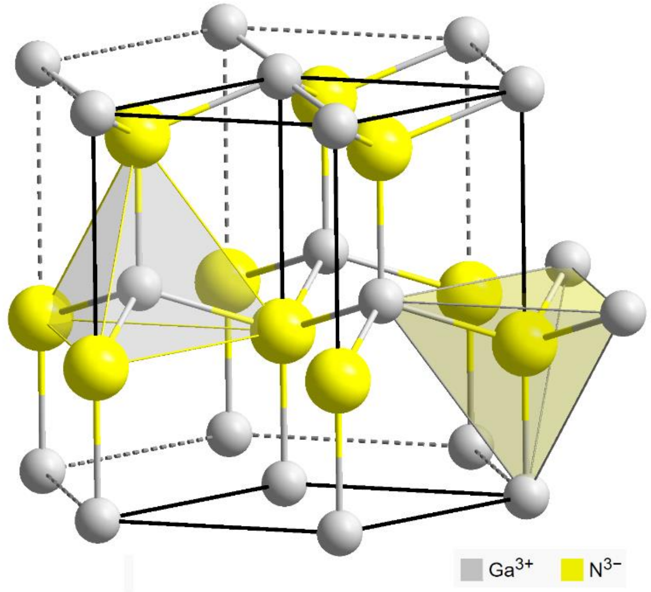
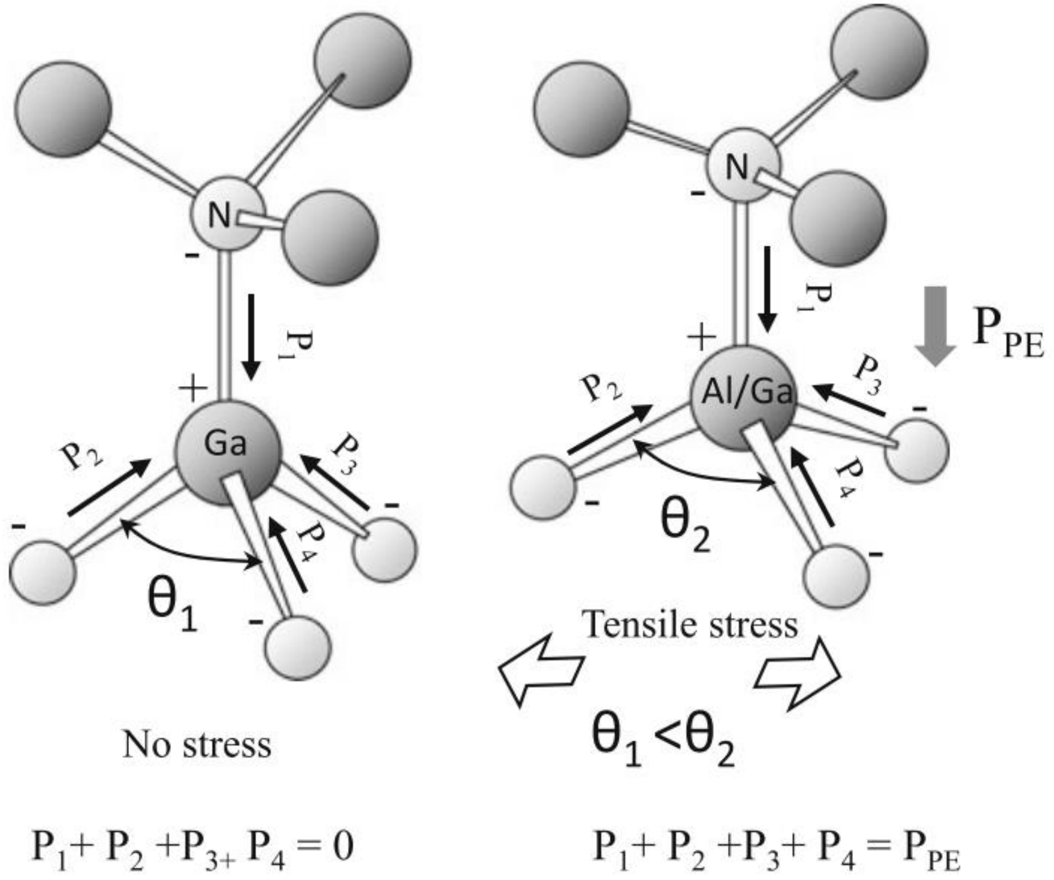
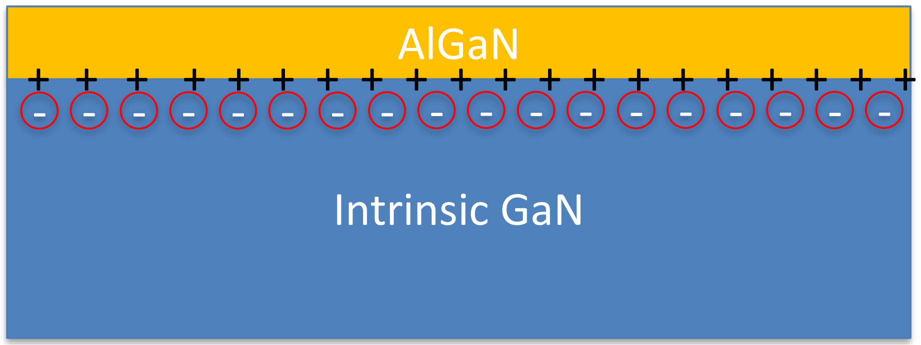
What is GaN



- Wurtzite crystal structure
  - Piezo electric
  - High breakdown electric field: 10X than Si
- Wide application in LED
  - High efficiency in illumination industry
  - Relatively cheap with high throughput MOCVD production.
- High electron mobility

GaN HEMT: high mobility and electron density





Achieving high electron density without extra doping. Achieving much lower Ron than Si

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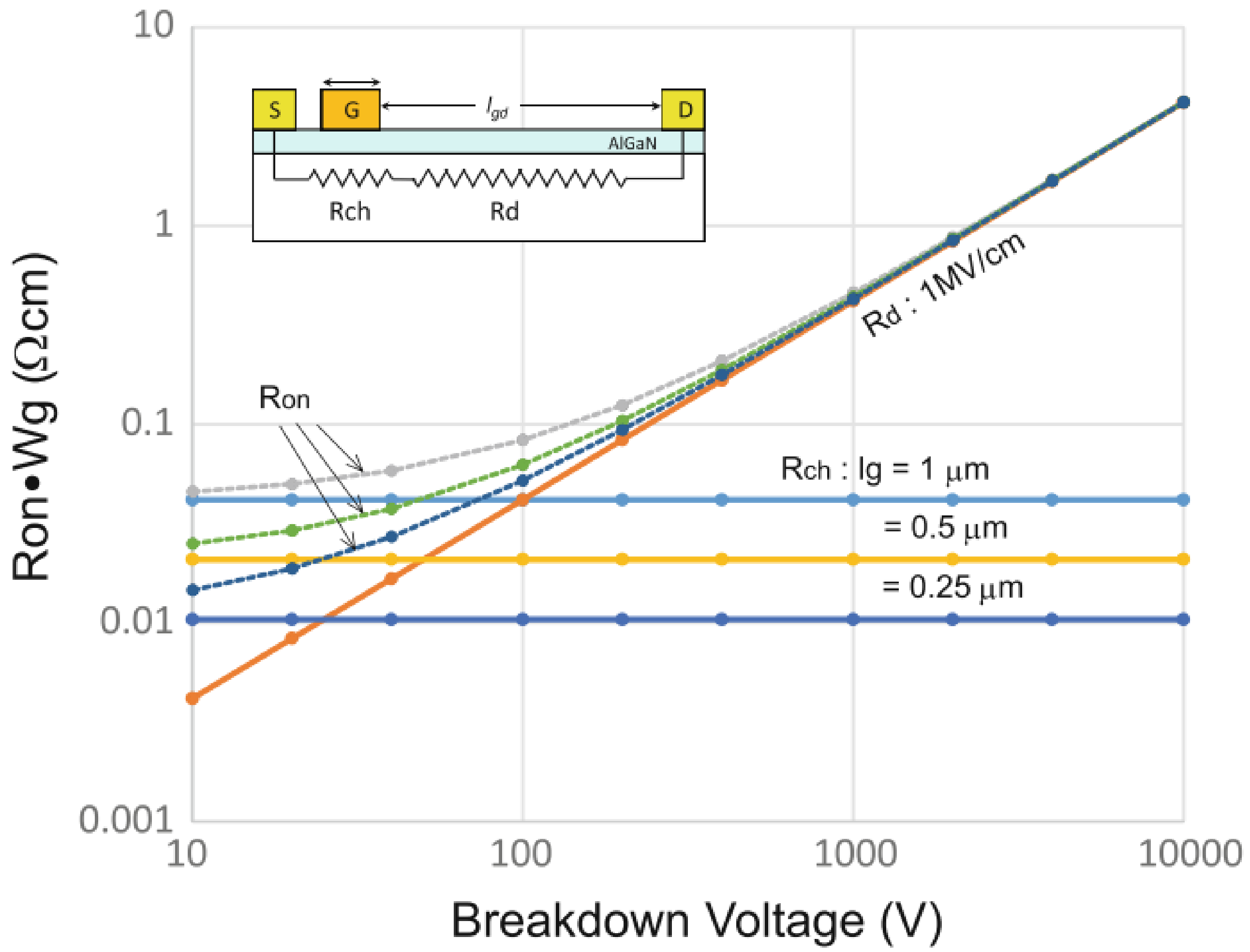
Normally off vs Normally on

- Connect to a Si normally off transistor
  - Bulky, lower efficiency
  - Current market solution
- Gate recess, ion doping or p-Gate
  - Deteriorate the mobility
  - Difficult to control
- No ideal commercial solution yet.

Ron vs Breakdown Voltage



Under specific application requirements, the voltage will be fixed. Then minimum Rd is fixed

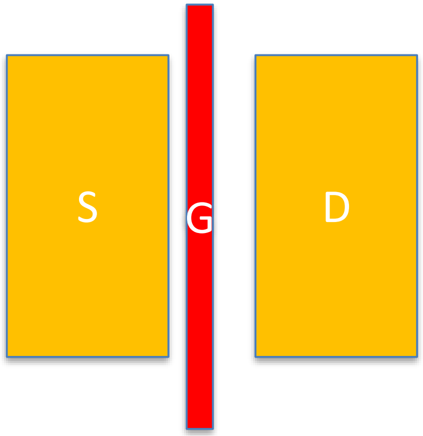
Capacitance vs Ron

Table 1.2 Typical scaling law, expected performance, and chip size

Device dimension is miniaturized by 1/k	
Blocking voltage	1/k
R_{on}	1
Capacitance	$1/k^2$
Chip area	$1/k^2$
Switching loss ($R_{on} \cdot Q_g$)	$1/k^2$
Chip cost	$1/k^2$

Table 1.3 Estimated device dimension to satisfy the demands by the application voltage, e.g., 12 and 100 V for three types of materials

Blocking voltage (V)	Required dimension		
	Si	SiC	GaN
12	400 nm	60 nm	60 nm
100	3.3 μm	0.5 μm	0.5 μm



Ron can be reduced by elongating the device, but will increase Gate capacitance

Meneghini, Matteo et al. Power GaN Devices, 2012

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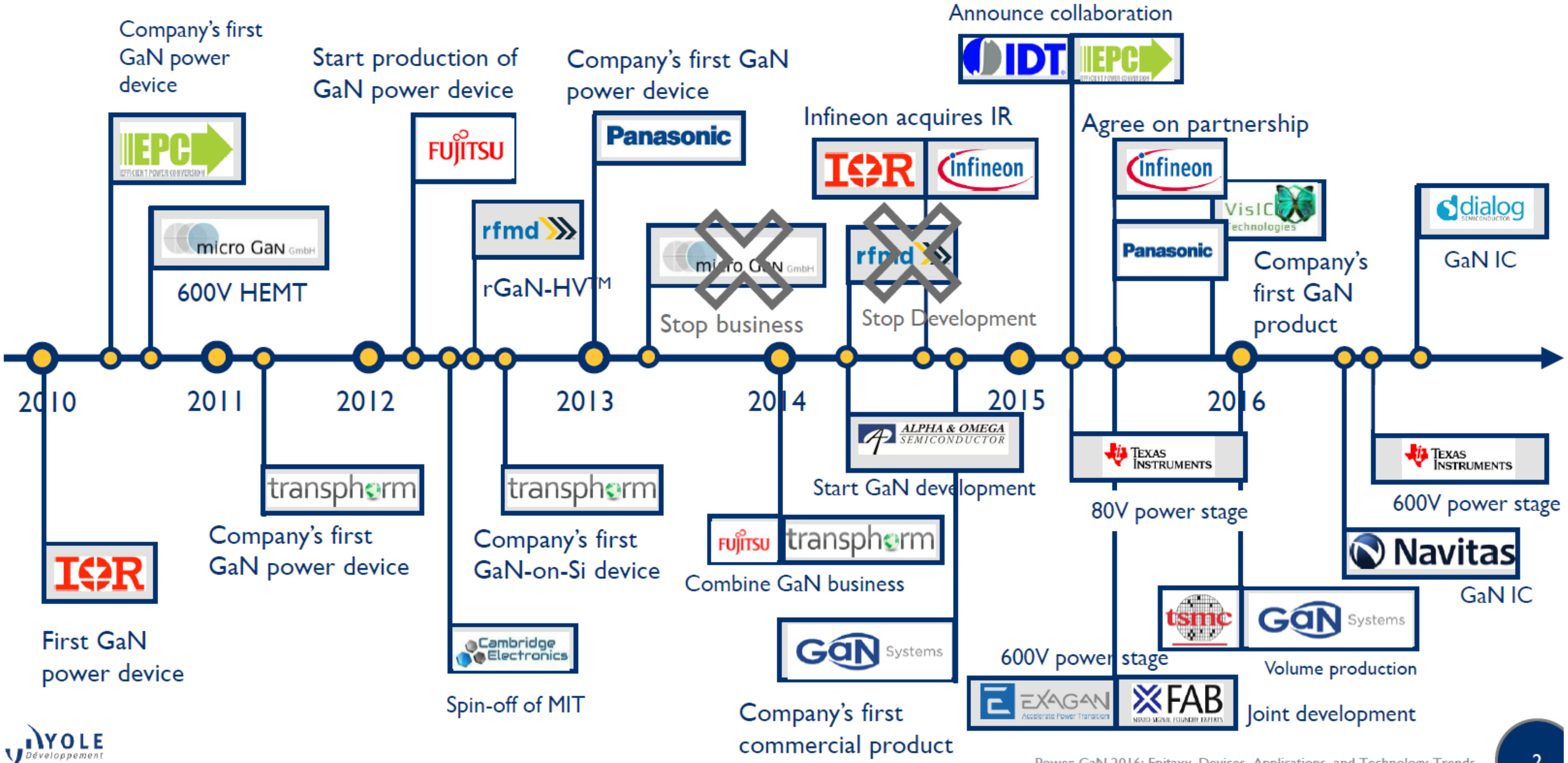
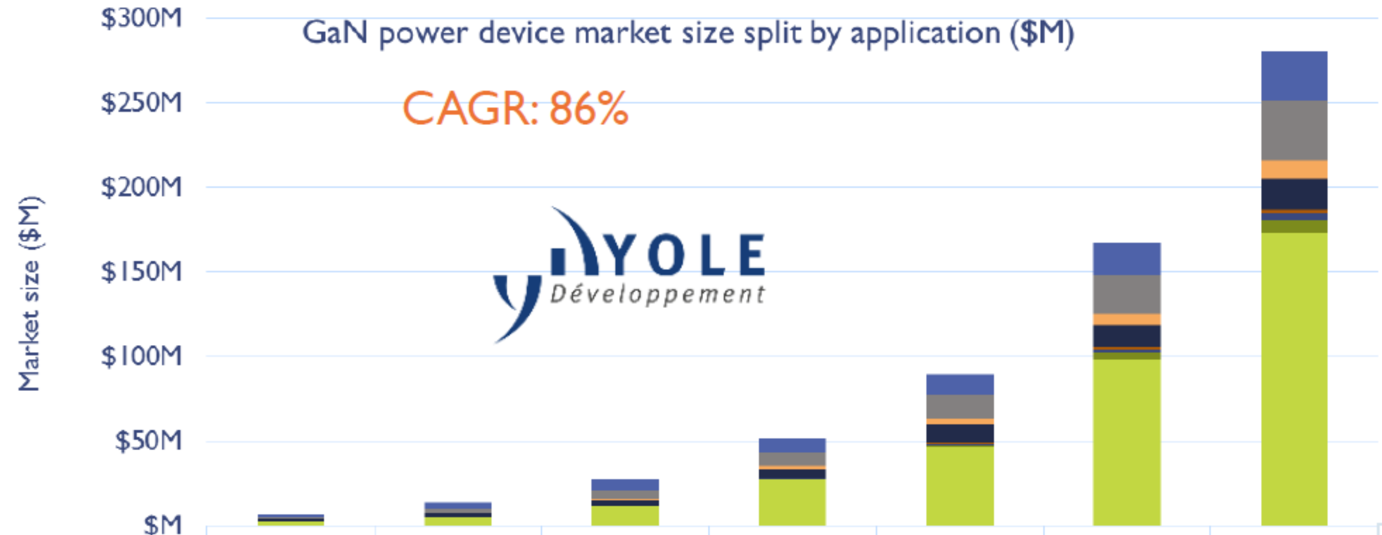
GaN technology development



Market growth



	2015	2016	2017	2018	2019	2020	2021	CAGR 2015 - 2021
Others, Audio, medical, R&D …	$ 2.0 M	$ 4.0 M	$ 6.5 M	$ 8.5 M	$ 12.7 M	$ 19.0 M	$ 28.5 M	56%
Lidar	$ 0.9 M	$ 1.8 M	$ 4.7 M	$ 8.2 M	$ 13.8 M	$ 23.4 M	$ 35.8 M	85%
Wireless Power	$ 0.0 M	$ 0.1 M	$ 0.8 M	$ 1.7 M	$ 3.5 M	$ 6.5 M	$ 10.8 M	/
Envelop Tracking	$ 1.6 M	$ 2.7 M	$ 3.2 M	$ 5.3 M	$ 10.5 M	$ 13.1 M	$ 17.8 M	49%
UPS	$ 0.0 M	$ 0.0 M	$ 0.0 M	$ 0.0 M	$ 0.7 M	$ 1.3 M	$ 2.3 M	/
PV	$ 0.1 M	$ 0.3 M	$ 0.4 M	$ 0.6 M	$ 0.9 M	$ 1.6 M	$ 3.7 M	74%
EV/HEV (including Charger and DC-DC)	$ 0.0 M	$ 0.0 M	$ 0.0 M	$ 0.0 M	$ 0.9 M	$ 4.1 M	$ 7.9 M	/
Power Supply	$ 2.2 M	$ 4.7 M	$ 11.3 M	$ 27.4 M	$ 46.6 M	$ 98.4 M	$ 173.2 M	108%
Total	**$6.8 M**	**$13.6 M**	**$27.0 M**	**$51.6 M**	**$89.7 M**	**$167.5 M**	**$280.0 M**	

Highlights

- GaN is promising to solve the efficiency challenge in power transistors
- Engineering is challenging to solve the trade-offs
- Market is waiting for the breakthrough in this field.
- Cambridge Electronics is one of the leaders!